

CLAIMS:

1. Testing device for testing a phase locked loop having a power supply input, said testing device comprising:
 - a power supply unit for providing a power supply signal (V_{DD}) having a variation profile to the power supply input of the phase locked loop, wherein a width and height of said variation profile are formed in such a way, that the voltage controlled oscillator is prevented from outputting an oscillating output signal (U_{out})
 - a means for disabling a feedback signal to a phase comparator of the phase locked loop such that said phase locked loop is operated in an open loop mode, and
 - a meter for measuring a measurement signal of the phase locked loop, while said power supply signal is provided to the power supply input.
2. Testing device for testing a phase locked loop device according to claim 1, said phase locked loop (PLL) having phase comparator (10) and said phase comparator (10) having a feedback input (U_{fb}) and a reference input (U_{ref}), wherein
 - both said feedback input (U_{fb}) and said reference input (U_{ref}) are connected to ground.
3. Testing device for testing a phase locked loop device according to claims 1 or 2, comprising a periodic signal generator for providing a periodic input signal having the same frequency to said feedback input (U_{fb}) and to said reference input (U_{ref}).
4. Testing device for testing a phase locked loop device according to claims 1, 2 or 3, wherein said meter is adapted to measure a current (I_{DD}) provided to the power supply input, an output voltage (U_{out}) and/or an oscillator control voltage (U_{vco}) of the phase locked loop.
5. Testing device for testing a phase locked loop device according to claim 1, 2, 3 or 4, wherein said power supply unit is adapted to provide a periodic power supply signal (V_{DD}).

6. Testing device for testing a phase locked loop device according to claims 1, 2, 3, 4 or 5, wherein the power supply unit and the periodic signal generator are both adapted to provide periodic signals having the same frequency.

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7. Testing device for testing a phase locked loop device according to one of claims 1 to 6, wherein the power supply unit and the periodic signal generator are both adapted to provide periodic signals having a phase difference between the periodic power supply signal (V_{DD}) and the periodic input signal is equal to 0, $T/4$ or $3T/4$, T being a period of both said periodic power supply signal (V_{DD}) and said periodic input signal.

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8. Testing device according to claim 4, comprising

- a high pass filter for filtering the current (I_{DD}) provided to the power supply input, and
- an integrator for integrating the filtered power supply current (I_{DD}), wherein the integrated power supply current is indicative of a defective phase locked loop.

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9. Phase locked loop comprising a testing device according to one of the preceding claims.

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10. Method for testing a phase locked loop (PLL) having a power supply input, comprising the steps:

- operating the phase locked loop in an open loop mode
- providing a power supply signal (V_{DD}) having a variation profile to the power supply input of the phase locked loop, wherein a width and height of said variation profile are formed in such a way, that the voltage controlled oscillator is prevented from outputting an oscillating output signal (U_{out}), and
- measuring a measurement signal of the phase locked loop, while said power supply signal is provided to the power supply input of the phase locked loop.

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11. Method for testing a phase locked loop device (PLL-device) according to claim 10, wherein said variation profile of the power supply signal has a ascending edge, said ascending edge being short enough (T_{RISE}) to prevent the voltage controlled oscillator (VCO) from outputting an oscillating output signal (U_{out}).

12. Method for testing a phase locked loop device according to claim 10 or 11, wherein said variation profile of the power supply signal has a descending edge, said descending edge being short enough (T_{RAMP}) to prevent the voltage controlled oscillator (VCO) from outputting an oscillating output signal (U_{out}).
13. Method for testing a phase locked loop device according to claim 10, 11 or 12, said phase locked loop (PLL) having phase comparator (10) and said phase comparator (10) having a feedback input (U_{fb}) and a reference input (U_{ref}), wherein
- 10 - both said feedback input (U_{fb}) and said reference input (U_{ref}) are connected to ground.
14. Method for testing a phase locked loop device according to claim 10, 11 or 12, wherein said feedback input (U_{fb}) and said reference input (U_{ref}) receive an identical periodic input signal.
- 15 input signal.
15. Method for testing a phase locked loop device according to one of the preceding claims, wherein the measurement signal is a current (I_{DD}) provided to the power supply input, an output voltage (U_{out}) and/or an oscillator control voltage (U_{VCO}) of the phase locked loop.
- 20 locked loop.
16. Method for testing a phase locked loop device according to one of the preceding claims, wherein the power supply signal (V_{DD}) is a periodic voltage signal.
17. Method for testing a phase locked loop device according to claims 15 and 16, wherein the periodic power supply signal (V_{DD}) and the periodic input signal to the reference input (U_{ref}) have the same frequency.
- 25 wherein the periodic power supply signal (V_{DD}) and the periodic input signal to the reference input (U_{ref}) have the same frequency.
18. Method for testing a phase locked loop device according to claim 17, wherein a phase difference between the periodic power supply signal (V_{DD}) and the periodic input signal is equal to 0, $T/4$ or $3T/4$, T being a period of both said periodic power supply signal (V_{DD}) and said periodic input signal.
- 30 a phase difference between the periodic power supply signal (V_{DD}) and the periodic input signal is equal to 0, $T/4$ or $3T/4$, T being a period of both said periodic power supply signal (V_{DD}) and said periodic input signal.